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April 1991 **Proceedings of the fourth international conference on Architectural support for programming languages and operating systems**, Volume 19 , 25 , 26 Issue 2 , Special Issue , 4

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2 An experimental study of several cooperative register allocation and instruction scheduling strategies

Cindy Norris, Lori L. Pollock

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

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1 Avoidance and suppression of compensation code in a trace scheduling compiler

Stefan M. Freudenberger, Thomas R. Gross, P. Geoffrey Lowney

July 1994 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 16 Issue 4

Full text available: pdf(3.58 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Trace scheduling is an optimization technique that selects a sequence of basic blocks as a trace and schedules the operations from the trace together. If an operation is moved across basic block boundaries, one or more compensation copies may be required in the off-trace code. This article discusses the generation of compensation code in a trace scheduling compiler and presents techniques for limiting the amount of compensation code: avoidance (restricting code motion so that no compensatio ...

Keywords: SPEC89, instruction-level parallelism, performance evaluation, trace scheduling